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Development of A Portable Type I to III Lightning Surge Protective Device for Compact Structures

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***Abstract* - Lightning Surge protection of large structures is done under zonal concept due to the requirement of a system with high current handling capacity and low voltage protection level. Induction of transient voltage in the wiring system within the building is another reason for such. However, in the case of compact structures such as base transmission stations (BTS) of tower sites, outside broadcast vehicles (OBV), various stages of railway systems etc. there are no sufficient lengths in the wiring network for implementing SPDs in such zonal-segment scenario. Also due to the remoteness of most BTSs and need for regular and/or continuous usage of OBVs and railway systems, the time-consuming replacement of out-of-order fixed SPDs is most often not warranted. In this backdrop, it was proposed to develop a portable/pluggable system of coordinated SPDs with high current handling capacity and low voltage protection level. A compact SPD system that is capable of handling high currents (50 kA) with low let through voltage (1 kV) was designed using PSCAD and a thorough market research was conducted to identify products that satisfied the requirements of the system designed in PSCAD. Type I and III SPDs capable of handling 50 kA and 2.5 kA respectively, were identified and used for the hardware implementation of the system. Elimination of the type II SPD made the design more compact and better suited for applications at space-restricted locations**

Keywords—Coordinated Surge Protective Device, compact Structure Surge Protection, type I to Type III surge protective device

I. INTRODUCTION

A surge protective device (SPD) is designed to withstand a maximum impulse current (I_{imp} or I_{max}) while letting through the minimum possible voltage known as the voltage protection level (U_p) that will be seen by the protected device. However, due to various limitations the two parameters, I_{max} and U_p are complementary, i.e. as I_{max} increases U_p also increases. Irrespective of the I_{max} of an SPD, the load is protected only if the U_p of the SPD that it sees immediately is less than it's Impulse Withstanding Voltage (U_w). Usually U_p should be significantly lower than U_w to compensate for the voltage drops along connecting wires.

In order to fulfil this requirement, it is customary to install a series of coordinated SPDs at a given site. As it is shown in the diagram in Fig 1a the SPD3, which is a type III SPD has the lowest U_p value out of the three SPDs. The U_p value is selected based on U_w of the load. Example U_p = 0.6 kV. The maximum value of current I_3 that the SPD can withstand is also the lowest among the SPDs (ex: 3 kA). When the incoming impulse voltage appears across the line, SPD3 operates first as it has the lowest U_p value. As this voltage increases, the current through SPD3 increases keeping its voltage output a constant.

The voltage appearing across SPD2 is the addition of the V_3 and V_4. R_3 and L_3 are the resistance and inductance of the wire lengths between the two SPDs (maybe a couple of tens of meters). The coordination should be set in such a way that before I_3 reaches its maximum value, V_2 should exceed the operating voltage of the SPD2.

A similar operation takes place at SPD1, which could withstand the full lightning current if the correct specification for a given geographical location has been selected. The clamping voltage at the three SPDs is graphically presented in Fig 1b. The mathematical basis is given by the following equation (1)-(4).

$$V_2 = V_3 + V_4 \quad (1)$$

$$V_1 = V_2 + V_5 \quad (2)$$

$$V_4 = i(t)\, R_3 + L_3\, di(t)/dt \quad (3)$$

$$V_5 = i(t)\, R_2 + L_2\, di(t)/dt \quad (4)$$

V_3, V_2 and V_1 are approximately the Voltage Protection Level (Up) of SPD3, SPD2 and SPD1 respectively

The above scenario is well applicable to a significantly large utility; however, problems arise when the structure is small such as a railway signal station, BTS (base transmission station) of a telecommunication tower, or if it is movable such as an OBV (outdoor broadcasting vehicle) of television and broadcasting companies. In such cases, suitable wire lengths could not be found that can produce sufficient values for V_4 and V_5 to make the coordinated SPDs operate sequentially.

Another serious practical issue with regard to SPDs is the inability of critical service sectors to afford a long time of repairing or replacing SPDs, during which power supply to maintain the service needs to be interrupted. The situation is even worse where there is a requirement of continuous or emergency service [1]. Thus, a ready-made plug-in type SPD system is highly demanded.

The third issue is the cost of installation of SPDs to a fleet of structures where each structure is operated occasionally (not all at once). In the case of several leading television companies in Malaysia, which has about 10-12 OBVs, it is understood that at any given time only one or two of the vehicles are in operation. Thus, it is a waste of resources to install a comprehensive set of SPDs to all vehicles, which are usually parked without any power supply connected, most of the times. Thus a few plug-in/plug-out type SPD systems would serve the protection of the entire fleet of vehicles.

Under such backdrop a need for a portable coordinated SPD array is in high demand as many applications of the critical service sector demands it. Thus, in order to design the coordinated SPD array the authors have used the PSCAD software. A new element known as the High-Power Precision Resistive-Inductor (HPPR) was developed for the coordination of the SPD array. The newly built product was tested as per the IEC Standards [2-4] to check for its performance.

II. METHODOLOGY

The procedure that led to coordinated surge protective devices is divided into 3 major categories: development by simulation, market analysis and hardware implementation and validation.

The simulation phase includes the simulation through software and the computational analysis (mathematical basis) for the product. All data samples obtained during the software simulation and computational analysis were recorded and compared for compatibility.

During the market analysis, the simulated SPD array and the components required was researched. The cost and the technical specifications were taken in to account during this phase. When the market analysis was successful the required components were bought for implementation. However, in case the components were not compatible with the pre-determined budget of the product and/or it does not meet the technical specifications required, the outcome was re-simulated with modifications.

The SPDs implemented were tested under type I and type III tests. Type I hardware test was not conducted due to the inaccessibility of the research team to a 10/350 µs impulse generator. Fig 2 illustrate the methodology in a flow chart.

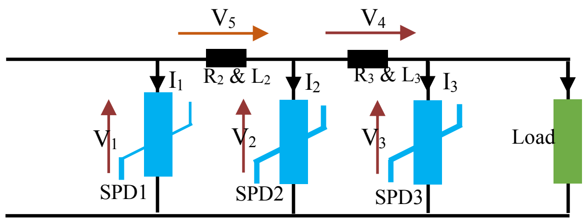


Figure 1a: Surge Protection Device Coordination

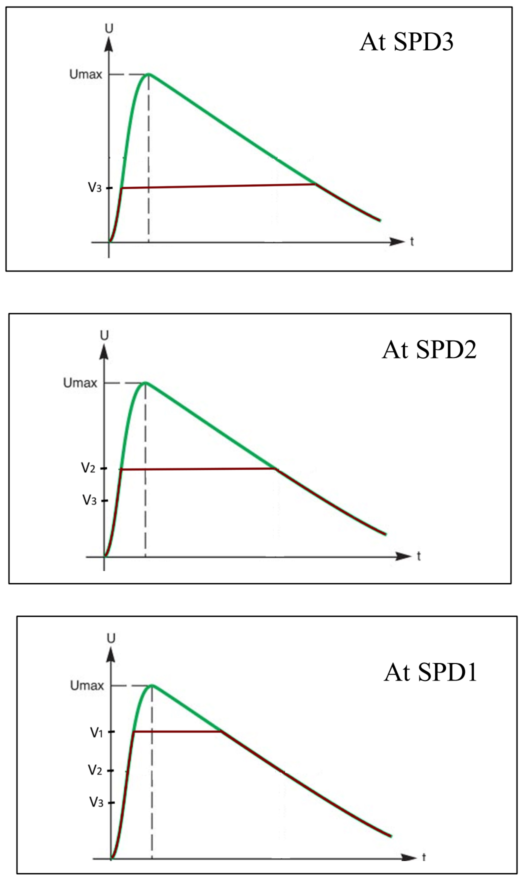


Figure 1b: Clamping of the voltage at each SPD

A. *Simulation Phase*

The preliminary design will include SPD arrays connected as per the standards. Thus, it is basic and under optimized.

The computational analysis includes the identification of the linear resistance and inductance of a length of 30m cable as this length is the minimum requirement, as per the IEC standards, need for the coordination of the SPDs. Further, the voltage drop between each pair of SPDs is calculated with the aid of the given equations.

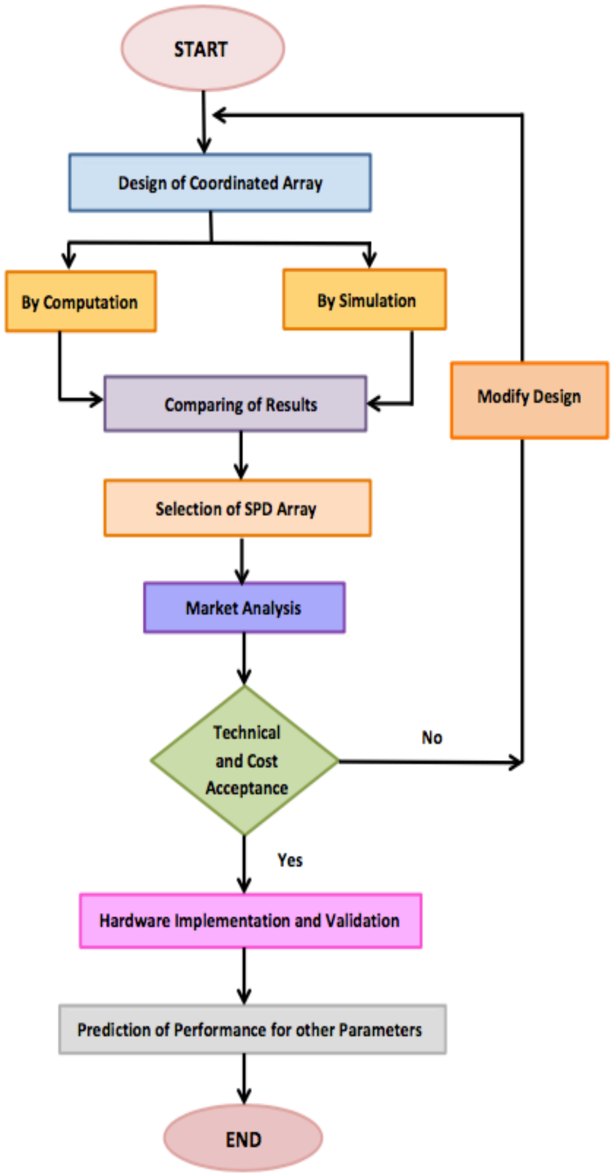


Figure 2: Flowchart of the method

A simulation will be conducted using the PSCAD software. The components such as SPDs, resistors and inductors are inclusive in the PSCAD library, where the ratings have to be given for each component. The SPD ratings for the preliminary design was selected with reference to the typical values for Type I, Type II and Type III SPDs. The typical values were selected by taking the U_w values of possible equipment and components that could be powered from an MSB (Main Switch Board), SSB (Sub Switch Board) and DB (Distribution Board). Other components such as inductors and resistors, parameter values were chosen with regard to the given equations and the results from the computational analysis (whichever value that is best suited). Further optimization was done once the simulation results were obtained.

B. *Market Analysis*

The results obtained at the end of simulations gives parameter values for SPDs of each type, the inductors and resistors. Thus, a thorough market research was needed to be done to identify the component availability. Surge Protective Devices with the necessary technical specifications were searched among the reputed SPD brands in the world.

All components were subjected to technical specifications and cost. In the event that components were not found under the required cost and technical specifications, the design was modified even further, and the virtual design phase was reconvened. When the components are found with the required technical specifications and cost, all components were acquired.

C. *Hardware Implementation and Validation*

The acquired SPDs and components were connected accordingly, and the newly built SPD was tested with the aid of a combinational waveform generator of capacity 30 kV (1.2/50μs) / 20 kA (8/20 μs). The validation considered the results of the simulation and hardware testing to compares them for the similarities in U_p values.

III. RESULTS AND DISCUSSION

i. *Preliminary Design*

The preliminary set of coordinated SPDs was constructed by the conventional Type I, II, III SPD components. The final simulation model determined the U_p for each type of SPD as 2.5 kV, 1.5 kV and 1 kV respectively. The market analysis that followed the simulation concluded that whereas the SPDs and other components for the required technical specifications were available, the cost of the SPDs and other components exceeds the pre-determined budget. Thus, a further modification of the SPD array was required for the SPDs to be within the budget constraints. Figure 3 illustrates the Type I, II, III SPD system.

ii. *Modified Design*

The modified design was developed without the type II SPD. Thus, the cost of the system was reduced to a reasonable value. Elimination of the type II SPD caused the design of the new array to be more complex that required a custom-made coordinating element (High Power Precision Resistive-Inductor; HPPR). The type I SPD consist of a U_p value of 1.3 kV and the type III SPD consists of a U_p value of 1 kV.

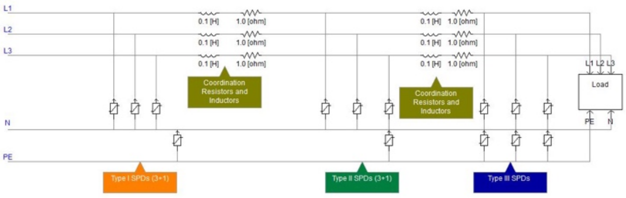


Figure 3: Coordinated Type I, II, III SPD system

iii. Virtual Design of Type I to III SPD

1. Computational Analysis

The computational analysis was conducted to determine the resistance and inductance of a 30 m length of wire. The wire typically used in these electrical systems is copper, which has a resistivity of 1.68 x 10^{-8} Ωm, and the diameter of the wire was assumed to be 1.6 mm. Thus, an assumption was made that the conductor carries a maximum current of around 24 A during the continuous operation. This assumption was made on the basis that the SPD array is developed for small structures. Equation (5) determined the resistance for the specific wire length as 0.25 Ω. Using (6) the self-inductance was determined as 4.89 μH for the 30 m copper wire.

$$R = \frac{\rho l}{A} \tag{5}$$

R: Resistance, ρ: resistivity of wire, A: Area of wire
l: Length

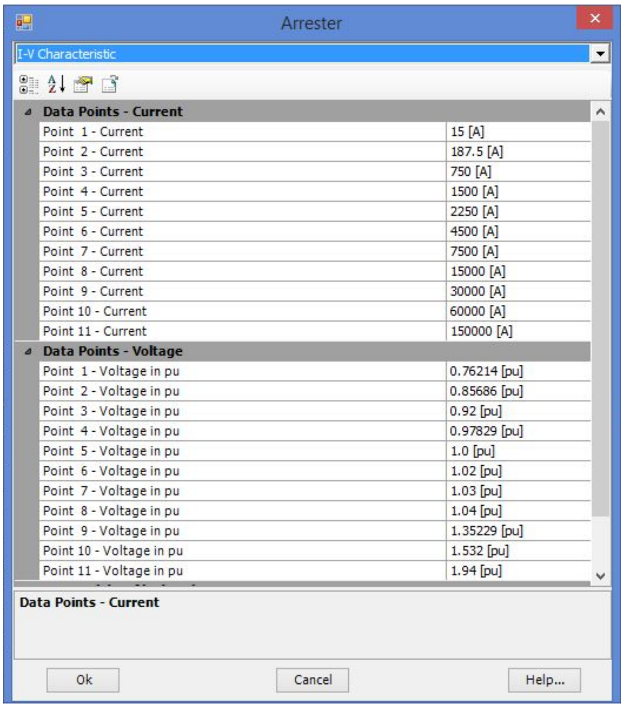
$$L = 2l\left\{\ln\left(\left(\frac{2l}{d}\right)\left(1+\sqrt{1+\left(\frac{d}{2l}\right)^2}\right)\right)-\sqrt{1+\left(\frac{d}{2l}\right)^2}+\frac{\mu}{4}+\left(\frac{d}{2l}\right)\right\} \tag{6}$$

l: length of wire, d: diameter of the wire, μ: permeability

However, the activation of the type I SPD only required a 300 V drop across the coordinating elements. As the difference between Up values of type I and III is 300 V, a computation was carried out with regard to equation (5) & (6) to determine the optimum resistance and inductance for a 300 V drop. The results obtained showed that lower values of resistance and inductance are required to cause a 300 V drop across the elements compared to the previously calculated values for a 30 m-wire length. Therefore, the computational values obtained through equation (5) & (6) were used in coordinating the SPDs and in both in the subsequent simulation as well as obtaining design parameters for the High-Power Precision Resistive-inductor (HPPR) in hardware implementation.

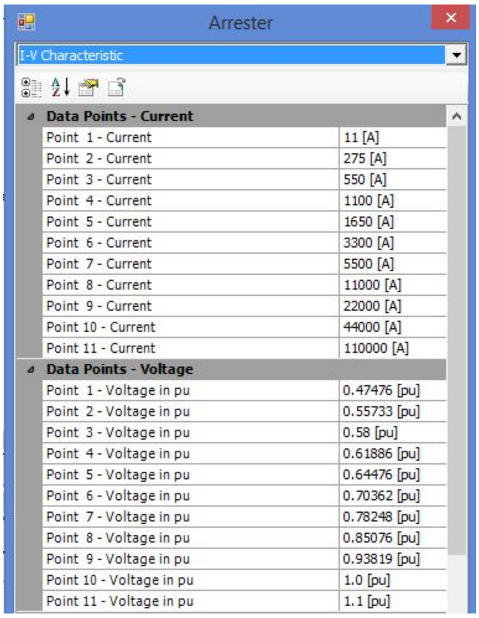
2. Software Simulation

Software simulation was conducted with the aid of PS-CAD. The 1st step of the simulation was performed by generating a SPD module. SPD module for type I and type III was created with the I-V characteristics as shown in Fig 4 and Fig 5.



Data Points - Current	
Point 1 - Current	15 [A]
Point 2 - Current	187.5 [A]
Point 3 - Current	750 [A]
Point 4 - Current	1500 [A]
Point 5 - Current	2250 [A]
Point 6 - Current	4500 [A]
Point 7 - Current	7500 [A]
Point 8 - Current	15000 [A]
Point 9 - Current	30000 [A]
Point 10 - Current	60000 [A]
Point 11 - Current	150000 [A]
Data Points - Voltage	
Point 1 - Voltage in pu	0.76214 [pu]
Point 2 - Voltage in pu	0.85686 [pu]
Point 3 - Voltage in pu	0.92 [pu]
Point 4 - Voltage in pu	0.97829 [pu]
Point 5 - Voltage in pu	1.0 [pu]
Point 6 - Voltage in pu	1.02 [pu]
Point 7 - Voltage in pu	1.03 [pu]
Point 8 - Voltage in pu	1.04 [pu]
Point 9 - Voltage in pu	1.35229 [pu]
Point 10 - Voltage in pu	1.532 [pu]
Point 11 - Voltage in pu	1.94 [pu]

Figure 4: Type III SPD I-V characteristics



Data Points - Current	
Point 1 - Current	11 [A]
Point 2 - Current	275 [A]
Point 3 - Current	550 [A]
Point 4 - Current	1100 [A]
Point 5 - Current	1650 [A]
Point 6 - Current	3300 [A]
Point 7 - Current	5500 [A]
Point 8 - Current	11000 [A]
Point 9 - Current	22000 [A]
Point 10 - Current	44000 [A]
Point 11 - Current	110000 [A]
Data Points - Voltage	
Point 1 - Voltage in pu	0.47476 [pu]
Point 2 - Voltage in pu	0.55733 [pu]
Point 3 - Voltage in pu	0.58 [pu]
Point 4 - Voltage in pu	0.61886 [pu]
Point 5 - Voltage in pu	0.64476 [pu]
Point 6 - Voltage in pu	0.70362 [pu]
Point 7 - Voltage in pu	0.78248 [pu]
Point 8 - Voltage in pu	0.85076 [pu]
Point 9 - Voltage in pu	0.93819 [pu]
Point 10 - Voltage in pu	1.0 [pu]
Point 11 - Voltage in pu	1.1 [pu]

Figure 5: Type I SPD I-V characteristics

Once the SPD blocks were generated, each block was connected as shown in Fig 8. In most cases, SPDs were modelled with double exponential functions, as per the literature survey. Thus, the beginning of this experimental procedure also consists of a double exponential function to identify the behaviour of the system. The double exponential function is illustrated in equation (7) and the PSCAD implementation of the equation is given in Fig 6 [5].

In order to obtain results with better accuracy, the Heidler function was used consequently. The Heidler function is illustrated in equation (8) and the PSCAD representation is shown in Fig 7. Test circuit shown in Fig 8 was used for both 8/20 and 10/350 waveform simulations.

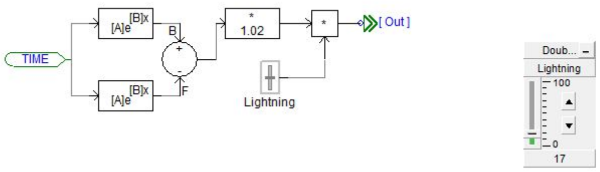


Figure 6: Double exponential curve generated in PSCAD

$$i = imax\,\eta\ \exp(-\alpha t) - \exp(-\beta t) \qquad (7)$$

η: correction factor, α: rise time, β: decay time

$$i = \frac{imax}{\eta}\,\frac{\left(\frac{t}{T}\right)^n}{1+\left(\frac{t}{T}\right)^n}\,\exp\left(-\frac{t}{\tau}\right) \qquad (8)$$

T: front time coefficient, τ: decay time coefficient
η: correction coefficent, n: exponent coefficient
t: time parameter

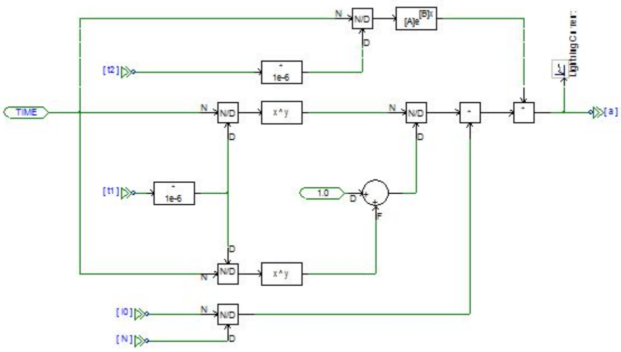


Figure 7: Heidler function Block in PSCAD

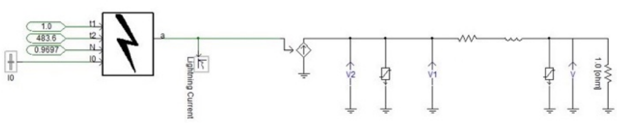


Figure 8: Complete simulation system block with Heidler function as the current source (testing of 8/20 and 10/350)

Test circuit in Fig 8 is injected with 10kA, 8/20 µs current waveform (Fig 9). The results show that the current across the type III SPD is less than 1 kA. The excess current flows through type I SPD (Fig 10 & Fig 11). Further, the let though voltage across the load and type III SPD is less than 1 kV (Fig 12). The 3 kA/ 6 kV (8/20, 1.2/50) waveform was used for the testing of the type III SPD (Fig 14,15,16,17) and the new SPD array showed results expected and performed better than a stand-alone type 3 SPD (let through voltage was around 0.8 kV at the load) and only a fraction of the total current was passed through the type III SPD.

Type I SPD required the 10/350μs test and was conducted with the same test circuit in Fig 8. A current of 50 kA was injected to the circuit. The 50kA was determined as the ideal current as it is the I_{imp} of the type I SPD. Results of the test show that the voltage across the load and type III SPD is 1kV. This is the rated U_p of the type III SPD. The nominal current of the type III SPD is 2.5 kA. Fig 18 illustrated the peak current of the type III SPD as 2.1 kA which is less than the nominal current of the SPD, hence, the SPD is not deteriorated by the injection of the large current, the remaining current in the system flows the type I SPD (Fig 21) as it coordinates with the type III SPD by using the HPPR and reaches its let though voltage of 1.3 kV (Fig 20).
Internal energy of the type III SPD is around 1.2 kJ under a 50 kA current injection. This is at an acceptable range for a type III SPD. Thus, will not fail due to internal energy built up.

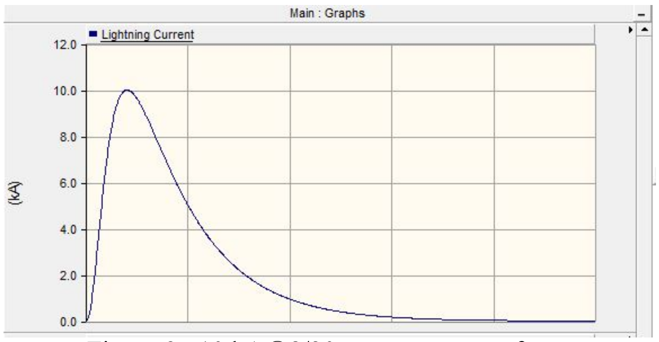


Figure 9: 10 kA@8/20 µs current waveform.

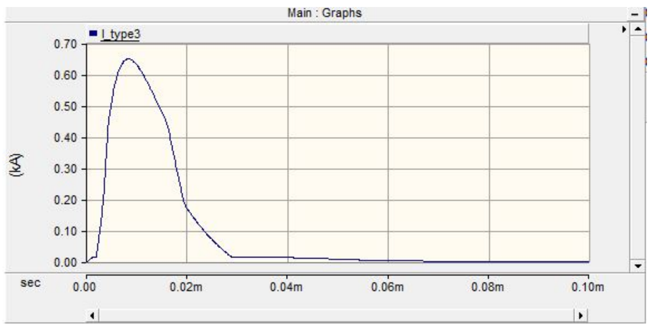


Figure 10: Current through Type III SPD (for 10kA@8/20)

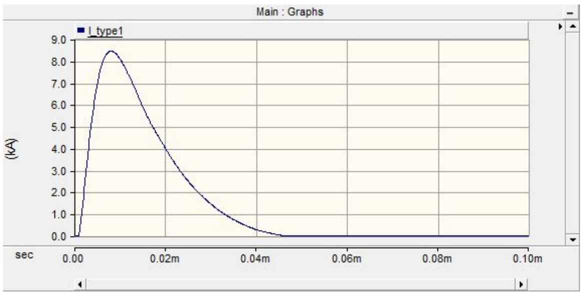


Figure 11: Current through Type I SPD (for 10kA@8/20)

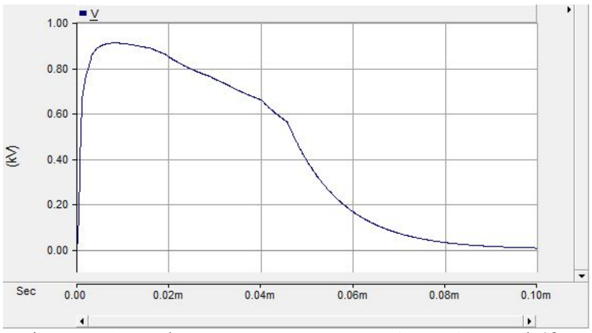


Figure 12: Voltage across Type III SPD & Load (for 10kA@8/20)

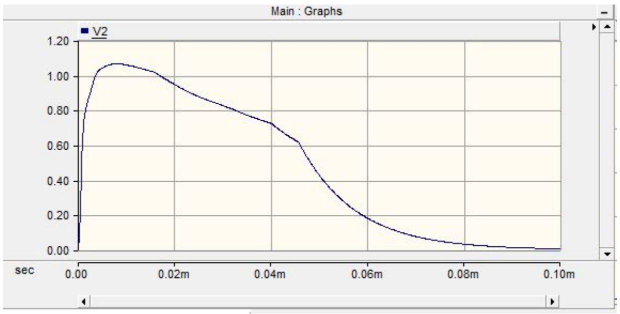


Figure 13: Voltage across Type I SPD (for 10kA@8/20)

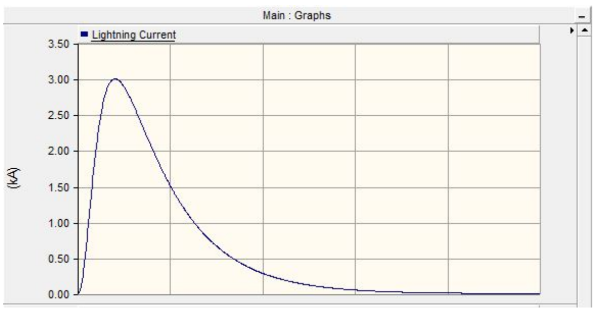


Figure 14: Lightning current 3 kA@8/20

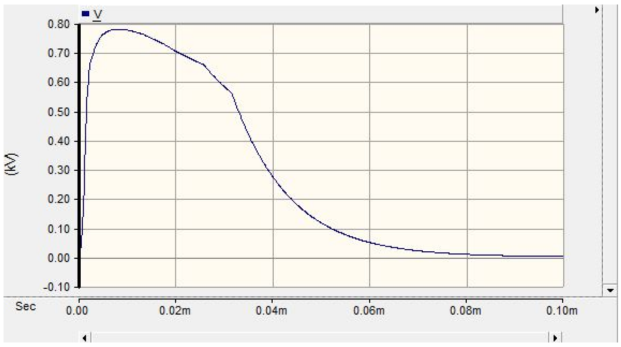


Figure 15: Type III SPD and Load voltage (for 3kA@8/20)

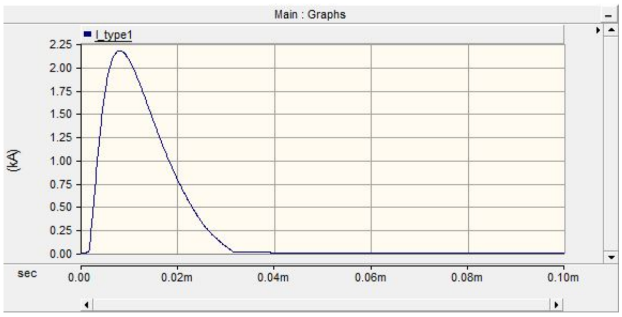


Figure 16: Current through Type I SPD (for 3kA@8/20)

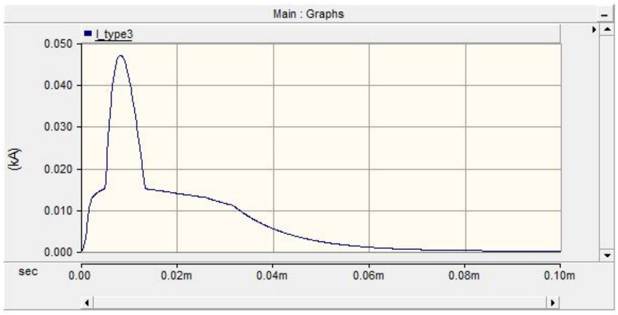


Figure 17: Current through Type 3 SPD (for 3kA@8/20)

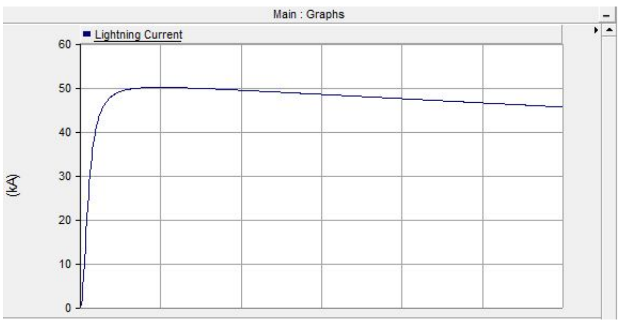


Figure 18: Lightning current 50 kA@10/350 µs waveform

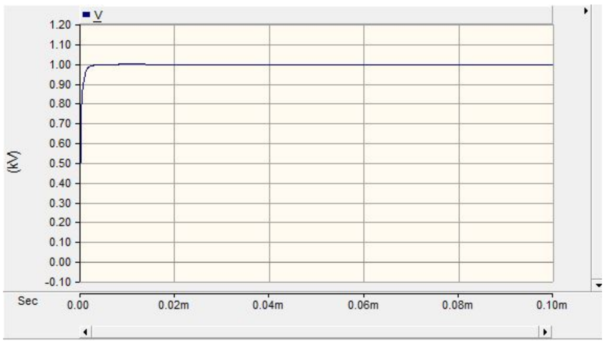


Figure 19: Type III SPD and load Voltage

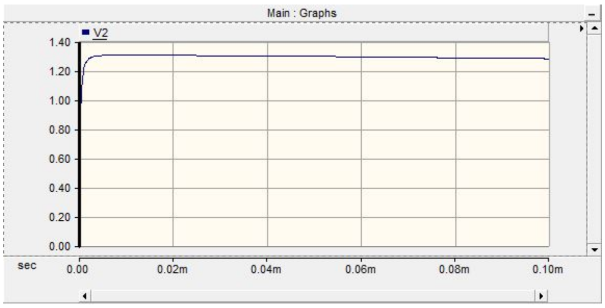


Figure 20: Voltage across type I SPD

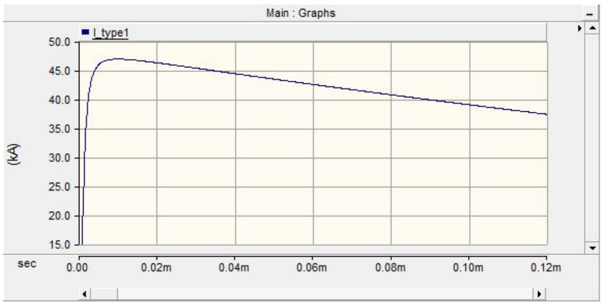


Figure 21: Current through Type I SPD

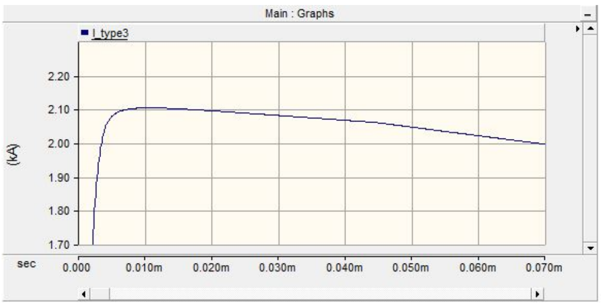


Figure 22: Current through Type III SPD

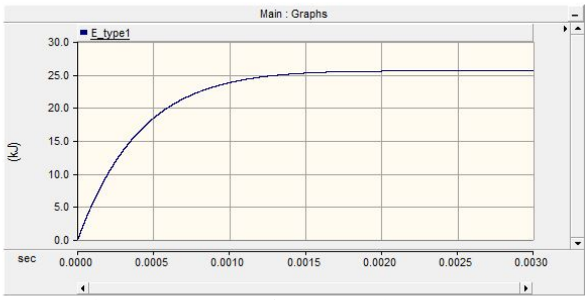


Figure 23: Internal energy of type I SPD

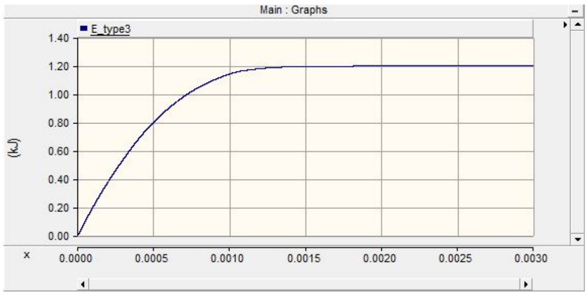


Figure 24: Internal energy of type III SPD

3. Market Analysis

Parameters found through computational and simulation analysis were favourable. Therefore, a market research was conducted to find components that are similar to the parameters of the SPD blocks.

A type I SPD capable of conducting a current I_{imp} of 50 III SPD capable of withstanding an I_{max} of 7 kA and U_p value of 1 kV. The basic parameters of type I and type III SPDs are given in table 1 and table 2 respectively. Both SPDs were purchased from the same manufacturer and they are the only manufacturers that produce type I SPDs with a U_p value of 1.3 kV.

Table 1: Type I SPD Specifications

Parameter	Value
Nominal Voltage (U_n)	230 V
Maximum Continuous Operating voltage (MCOV)	255V
Impulse current (I_{imp}) 10/350 µs	50 kA
Total impulse current (N-PE)	125 kA
Voltage Protective Level (U_p)	1.3 kA

Table 2: Type III SPD specifications

Parameter	Value
Nominal Voltage (U_n)	230 V
Maximum Continuous Operating Voltage (MCOV)	255 V
Nominal current (I_n)	2.5 kA
Max discharge current (I_{max})	7 kA
Rated load current	20 A
Voltage Protective Level (U_p)	1 kA

4. Hardware Implementation and Validation

The combinational waveform generator could display only the input current waveform and the final output voltage waveform (Fig 25, Fig 26).

The developed product was tested according to the IEC standard test regulations for type III SPD with 3 kA/6 kV combinational waveform and the breakdown occurred just under 1 kV as shown in Fig 25. It should be mentioned; even though the normal current discharge of the type III SPD is 2.5 kA, it is capable of discharging a maximum current of 6 kA. Thus, 3 kA discharged during the test can be handled by the type III SPD even if the type I SPD is not active. Therefore, even though the product passed the test it is inconclusive on whether the coordination worked accordingly.

In order to identify the coordination response of the system, a 10 kA/20 kV amplitude waveform were produced to test the product. Unlike the 3 kA/6 kV waveform, the 10 kA/20 kV peak 8/20, 1.2/50 waveform cannot be handled by the type III SPD alone as the maximum current handling capability of the type III SPD is 6 kA. Therefore, if the coordination fails the type III SPD will need replacement due to internal damage.

When the test waveforms were applied the load, voltage was clipped at just over 1 kV due to the type III SPD and as the Fig 26 illustrates, the 10 kA current was sent to ground through the SPD array. After the completion of the tests neither of the 3 type III SPDs showed any sign of deterioration (L-L SPD). Therefore, it gives conclusive proof that the new coordinated SPD array is functional and performs at an optimum level

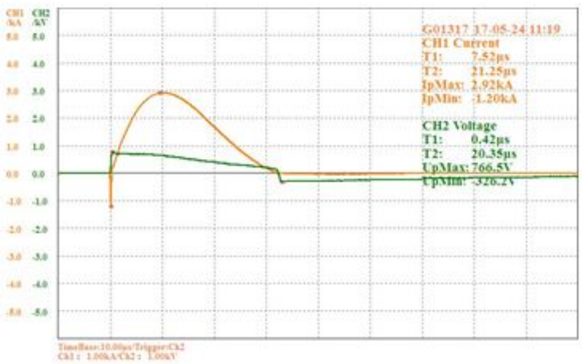


Figure 25: 3 kA/6 kV @8/20 and 1.2/50 µs combinational waveforms

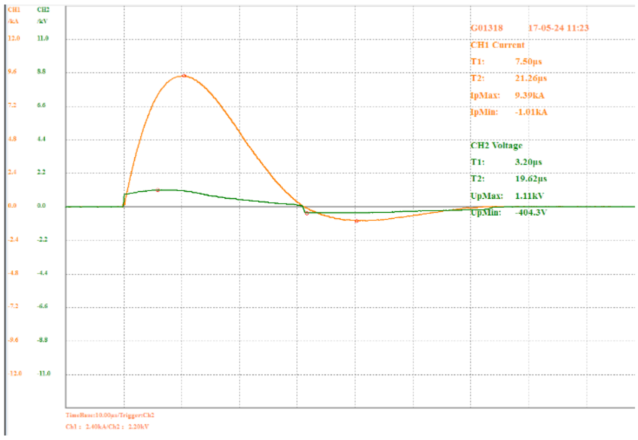


Figure 26: 10 kA/20 kV @ 8/20 and 1.2/50 µs combinational waveforms

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Based on the performance of the product under the combinational waveform generator testing, it can be shown that the simulation results and the hardware test results are almost identical in U_p value. Therefore, a favourable outcome for the 10/350 µs waveform test can be predicted as simulation test results are favorable.

4. Development of High Power Precision Resistive-inductor (HPPR)

The coordination of transients requires elements that are capable of handling large currents with low insertion losses, voltage drops and changes in element parameters once subjected to changes in temperature [6]. Under these circumstances, an element with hybrid capabilities of a NTCR and a precision resistor that is capable of withstanding high currents were required. Hence, the HPPR was developed. It is tested for high power surge withstanding capabilities and consists of negligible insertion loss for the nominal frequency of 50 Hz. Voltage loss due to the insertion of the HPPR was tested and it performs at a level of 1 V drop per 10 A of current. The temperature effect on the element is negligible, in the sense that it performs as precise as a precision resistor but has the ability to handle currents of the kA range.

Many applications of SPDs at space restricted structures, such as radio base stations close to communication towers, need miniatured components [7]. In this regard the HPPR developed in this study is still at a disadvantage as the end-product is bulky, although the weight is not a concern. This drawback will be minimized in the next phase of development.

IV CONCLUSIONS

A compact, easily pluggable, Type III to I SPD has been developed by inserting a High-Power Precision Resistive-inductor in between a Type I and Type III SPD. The Coordinated SPDs and the electrical parameters of the HPPR were selected by design simulation carried out with the aid of ANSYS software. The physical components for the HPPR were selected through a market survey. The SPD unit developed was tested for 8/20 µs current impulse and combinational waveform. The response of the unit for 10/350 µs current waveform has been studied by simulation. The unit has many applications in the industrial and commercial sector.

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